Course Type	Course Code	Name of Course	L	T	P	Credit
DE	NECD520	DSP Integrated Circuits	3	0	0	3

Course Objective

The objective of this course is to impart knowledge on

- Analyze the mapping of DSP algorithms onto hardware
- Synthesize different DSP architectures and Processing Elements

Learning Outcomes

Upon successful completion of this course, the students will:

- Understand the different architectures in Digital Signal Processor
- Implement DSP algorithm in processor
- Build large DSP systems
- Develop Multirate sampling-based signal processing applications.
- Analyse the different processing elements in DSP IC

Unit No.	Topics to be Covered	Lecture Hours	Learning Outcome
1	FFT Processor, Design Iteration Scheduling, Loop-Folding, Cyclic Scheduling Formulation, Overflow and Quantization, Scheduling Algorithms, FFT Processor, Resource Allocation, Partitioning and Assignment Interpolator, Processor, Memory Assignment Butterfly Processor DCT Processor	07	Understanding the concept of DSP system
2	DSPs and microprocessors, embodiment, alternatives, memory architecture, addressing, pipelining, on-chip, debugging, power consumption and management, clocking, application support, choosing processor architecture rends. Standard digital signal processors, Application specific IC's for DSP.	08	To get the exposure on DSP based processor
3	Standard DSP and Ideal DSP architectures, Multiprocessors and multicomputer, message-based architectures, Systolic and Wave front arrays, Shared memory architectures. SHARC and Blackfin processors – Architecture, overview, memory management, I/O management, On chip resources, programming considerations, Real time implementations.	09	To get the knowledge on architecture of digital signal processors
4	Mapping of DSP algorithms onto hardware, Uniprocessor architectures, Isomorphic mapping of SFGs, Implementation based on complex PEs, vector-multiplier based implementations, numerically equivalent implementation, implementation of WDFs, Shared memory architecture with Bit – serial PEs, building the large DSP systems, Single Instruction Computer (SIC).	09	To understand the concept of synthesis part on DSP architecture
5	Bit-Serial Arithmetic, Bit-Serial Two-Port Adaptor 8 S/P Multipliers with Fixed Coefficients Minimum Number Of Basic Operations, Bit-Serial Squares, Serial/Serial Multipliers, Digit-Serial Arithmetic, Cordic Algorithm, Distributed Arithmetic, The Basic Shift, Accumulator, Reducing The Memory Size, Complex Multipliers, Improved ShiftAccumulator FFT Processor, Twiddle	09	To gain the knowledge on different processing elements in DSP ICs.

	Factor PE, Control PEs, Address PEs, Base Index Generator, Ram Address PEs.		
	Total	**42**	

Textbooks:

1. Lars Wanhammer, "DSP Integrated Circuits", Elsevier India Pvt. Ltd, New York, 2012.
2. Phil Lapsley, Jeff Bier, AmitSholam and Edward A.Lee, "DSP Processor Fundamentals-Architectures, and Features", Wiley India, reprint 2011.

Reference Books:

1. A.V.Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2013.
2. Steven W. Smith, "The Scientist and Engineer's Guide to Digital Signal Processing", 1998.
3. P.P.Vaidyanathan, Multirate Systems & Filter Banks, Prentice Hall, Englewood cliffs, NJ, 1993